## Multi-Chip Package MEMORY

**512M bit(1.8V ,64M x 8) SLC NAND Flash**
**256M bit(1.8V ,16M x 16) LPDDR(Mobile DDR) SDRAM**

| Revision No. | History | Draft Date | Remark |
|---|---|---|---|
| 00 | Initial Draft | Aug. 2012 | |
| 01 | -Page 2 : Data Rate from 333MHz to 333Mbps<br>-Page 55 ~ 57 : Electrical Characteristics and Recommended AC Operating Conditions change | Nov. 2012 | |

# Multi-Chip Package MEMORY

512M bit (x8,1.8V) NAND Flash and 256M bit (x16,1.8V) LPDDR SDRAM

**<MCP Features>**

❖. Operating Temperature : -25℃ ~ 85℃
❖. 107 ball FBGA Type - 10.5mmx13mm

**<NAND Features>**

- **Power Supply**
  -1.8V Device : 1.7V ~ 1.95V
- **Organization**
  -Memory Cell Array : (64M + 2M) x 8bits
  -Data Register : (512 + 16) x 8bits
- **Automatic Program and Erase**
  -Page Program : (512 + 16)Bytes
  -Block Erase : (16K +512)Bytes
- **Page Read Operation**
  -Page Size : (512 + 16)Bytes
  -Random Access : 15us(Max.)
  -Serial Page Access : 50ns(Min.)
- **Fast Write Cycle Time**
  -Program time : 200us(Typ.)
  -Block Erase time : 2ms(Typ.)
- **Copy-Back PROGRAM Operation**
  -Fast Page copy without external buffering
- **Command Register Operation**
- **Security features**
  -OTP area, 16Kbytes(32 pages)
- **Hardware Data Protection**
  -Program / Erase locked during Power transitions
- **Data Integrity**
  -Endurance : 100K Program / Erase Cycles
  (With 1bit/528byte ECC)
  -Data Retention : 10 years

**<LPDDR SDRAM Features>**

- **Density: 256 Mbits**
- **Organization**
  4Meg × 16 bits × 4 banks
- **Power supply:**
  - VDD / VDDQ = 1.7V ~ 1.95V
- **Data rate: 333Mbps**
- Differential clock inputs (CK and /CK)
- Bidirectional data strobe per byte of data
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Four internal banks for concurrent operation
- Data mask (DM) for write data – one mask per byte
- Programmable Burst Lengths: 2, 4 ,8 or 16
- Burst type: Sequential or interleave
- Clock Stop capability
- Concurrent Auto Precharge option is supported
- Configurable Drive Strength (DS)
- Auto Refresh and Self Refresh Modes
- Optional Partial Array Self Refresh (PASR) and Temperature Compensated Self Refresh (TCSR)
- Deep Power Down Mode (DPD)
- 1.8V LVCMOS-compatible inputs
- Status Read Register (SRR)
- 64ms refresh

## MCP Product Information

| Part number | NAND Flash | LPDDR SDRAM | Package |
|---|---|---|---|
| MST9B08B16FMHF-533E | 512Mbit (x8) – 1.8V | 256Mbit (x16) – 1.8V | FBGA 107 ball |

# PIN CONFIGURATION(107-FBGA)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| A | | DNU | | | | | | | DNU | DNU |
| B | DNU | NC | DQ0 | VDD | VSSn | VCCn | NC | A3 | NC | DNU |
| C | | VSS | DQ2 | DQ1 | CLE | CE# | A0 | A1 | A2 | |
| D | | VDDQ | DQ4 | DQ3 | ALE | WEn# | BA0 | BA1 | A10 | |
| E | | VSSQ | DQ6 | DQ5 | RE# | R/B# | RAS# | NC | CS# | |
| F | | VDDQ | LDQS | DQ7 | WP# | NC | CAS# | WEd# | VSS | |
| G | | VSS | LDQM | CLK# | NC | NC | A12 | CKE | VDD | |
| H | | VDD | UDQM | CLK | NC | NC | A8 | A9 | A11 | |
| J | | VSSQ | UDQS | DQ8 | IO0 | IO2 | IO4 | IO6 | A7 | |
| K | | VDDQ | DQ9 | DQ10 | NC | NC | NC | NC | A6 | |
| L | | VSSQ | DQ11 | DQ12 | IO1 | IO3 | IO5 | IO7 | A5 | |
| M | | VDD | DQ13 | DQ14 | NC | NC | NC | NC | A4 | |
| N | DNU | NC | DQ15 | VSS | VSSn | VCCn | VCCn | VSSn | NC | DNU |
| P | DNU | DNU | | | | | | | DNU | DNU |

Nand Flash

Mo-DDR

NC/DNU

# PIN DESCRIPTION -107-FBGA

### ❖512Mb(64Mb x 8) NAND Flash

| SYMBOL | DESCRIPTION |
|---|---|
| IO0~IO7 | Data Input / Output |
| CE# | Chip Enable |
| WEn# | Write Enable |
| RE# | Read Enable |
| ALE | Address Latch Enable |
| CLE | Command Latch Enable |
| WP# | Write Protect |
| R/B# | Ready/Busy out |
| VCCn | Power Supply |
| VSSn | Ground |

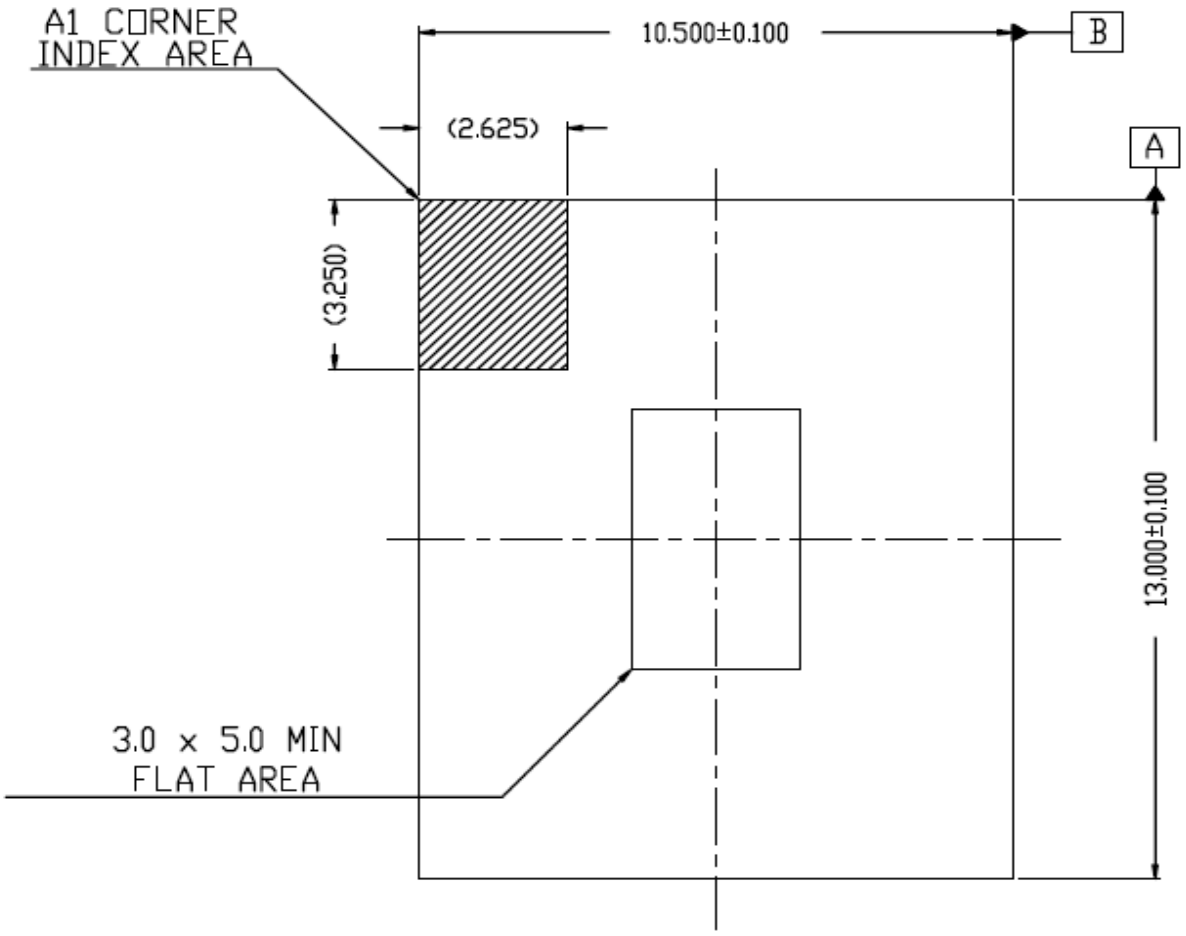
### ❖ 256Mb(16Mb x 16) LPDDR

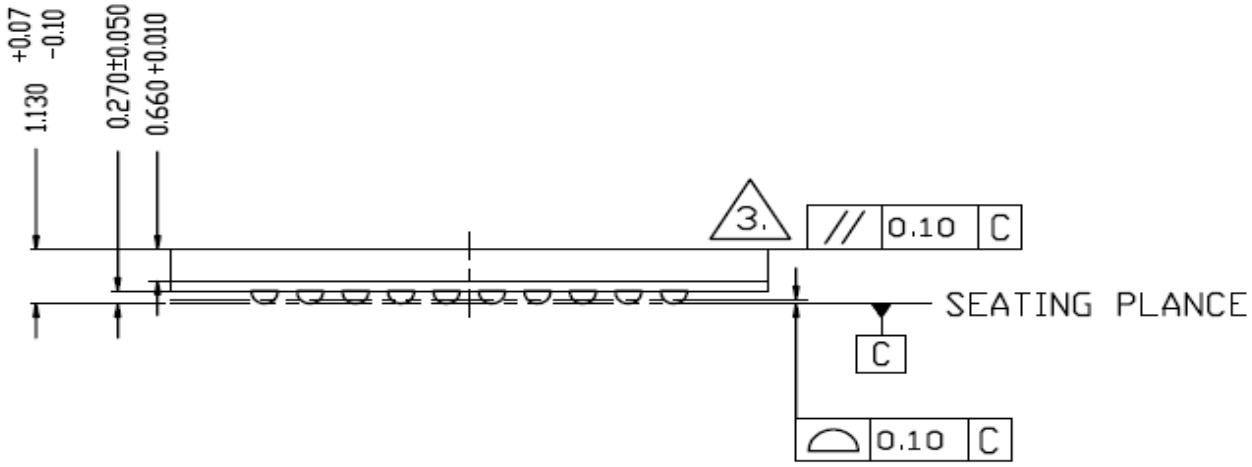
| SYMBOL | DESCRIPTION |
|---|---|
| A0~A12 | Address Inputs |
| BA0, BA1 | Bank Address Inputs |
| DQ0~DQ15 | Data Bus |
| CS# | Chip Select |
| RAS# | Row Address Strobe Command |
| CAS# | Column Address Strobe Command |
| WEd# | Write Enable |
| LDQM/UDQM | Input Data Mask |
| LDQS/UDQS | Data Strobe |
| CLK | Clock Input |
| CKE | Clock Enable |
| VDD | Power Supply |
| VDDQ | I/O Power supply |
| VSS | Ground |
| VSSQ | I/O Ground |

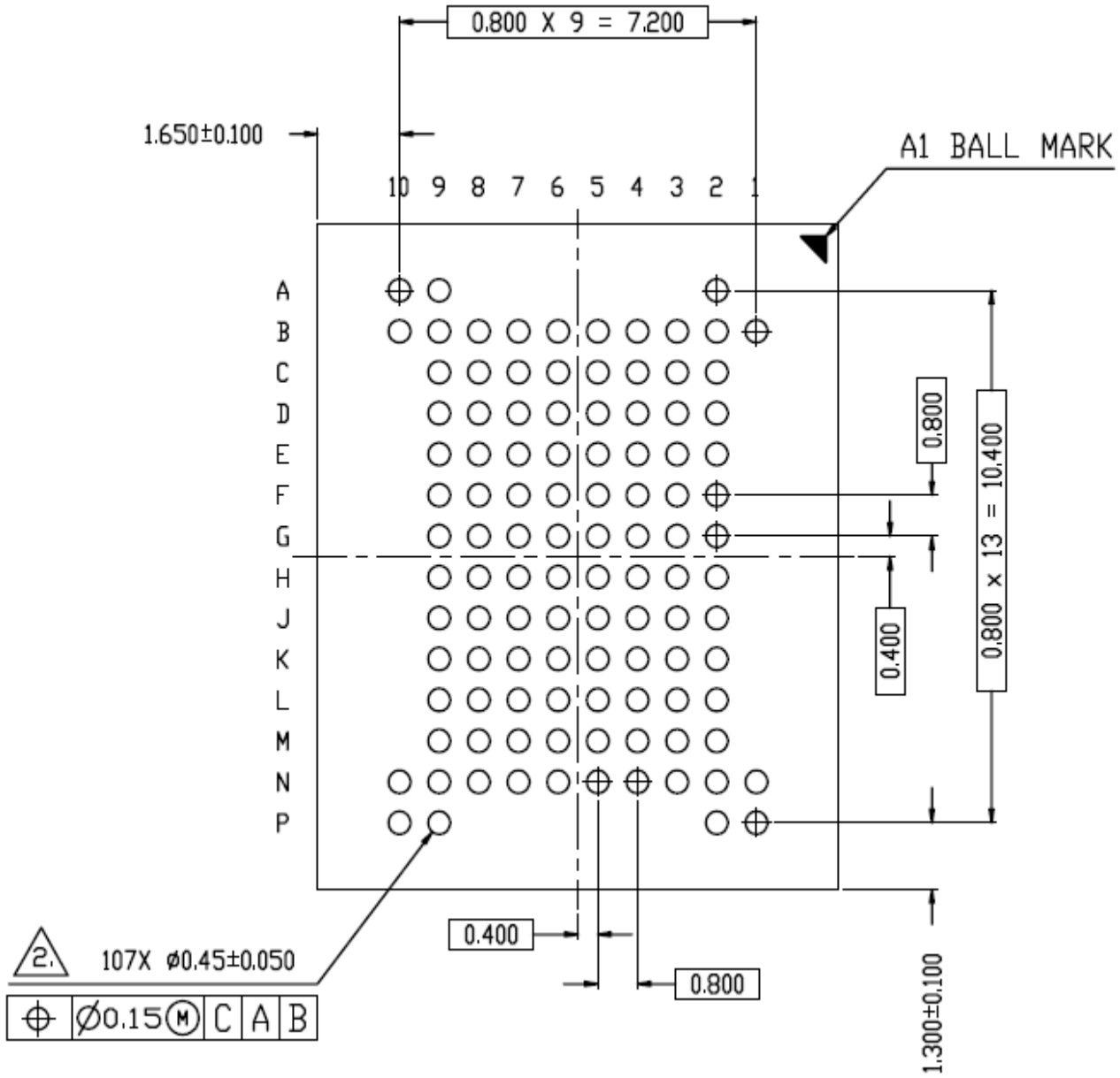
### ❖Common

| SYMBOL | DESCRIPTION |
|---|---|
| NC | No Connection |
| DNU | Do Not Use |

## FBGA 107 Ball 10.5 × 13 mm - package outline






NOTE:

1. ALL DIMENSIONS are in Millimeters.
2. POST REFLOW SOLDER BALL DIAMETER.
   (Pre Reflow Diameter : Ø0.40±0.02)
3. TOLERANCE INCLUDES WARPAGE.

## Ordering Information