Multi-Chip Package MEMORY
256M Bit (32Mx8) Nand Flash / 512M Bit (8Mx16x4Banks) DDR2 SDRAM

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>History</th>
<th>Draft Date</th>
<th>Remark</th>
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<tbody>
<tr>
<td>Rev00</td>
<td>Initial Draft</td>
<td>Dec, 2009</td>
<td>Preliminary</td>
</tr>
<tr>
<td>Rev01</td>
<td>Modified Ordering Information</td>
<td>Jun, 2011</td>
<td></td>
</tr>
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## MCP Product list

<table>
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<tr>
<th>Part number</th>
<th>NAND product</th>
<th>DDR2 SDRAM</th>
<th>Package</th>
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<tbody>
<tr>
<td>MST7A08D16DMFC-XXX</td>
<td>256 Mbit(x8) – 3.3V</td>
<td>512 Mbit(x16) – 1.8V</td>
<td>FBGA 104 ball</td>
</tr>
</tbody>
</table>
Multi-Chip Package MEMORY

256M Bit (32Mx8) NAND Flash / 512M Bit (8Mx16x4Banks) DDR2 SDRAM

<MCP Features>
- Operating Temperature : 0℃ ~ 70℃
- 104-ball FBGA Type -9.0mmx9.0mm,0.65mm pitch

<NAND Features>
- Power Supply Voltage : 2.7~3.6V
- Organization
  - Memory Cell Array : (32M + 1024K)bit x 8 bit
  - Data Register : (512 + 16)bit x 8bit
- Automatic Program and Erase
  - Page Program : (512 + 16)Byte
  - Block Erase : (16K + 512)Byte
- Page Read Operation
  - Page Size : (512 + 16)Byte
  - Random Access : 12μs(Max.)
  - Serial Page Access : 50ns(Min.)
- Fast Write Cycle Time
  - Program time : 200μs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Register Operation
  - Command Address/Data Multiplexed I/O Port
  - Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Data Integrity
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation

<DDR2 SDRAM Features>
- Density: 512M bits
- Organization
  - 8M words × 16 bits × 4 banks
- Power supply: 1.8V ± 0.1V
- Data rate: 800Mbps/667Mbps/533Mbps/400Mbps
- Four internal banks for concurrent operation
- Interface: SSTL_18
- Burst lengths (BL): 4, 8
- Burst type (BT):
  - Sequential (4, 8)
  - Interleave (4, 8)
- /CAS Latency (CL): 3, 4, 5, 6
- Precharge: auto precharge option for each Burst access
- Driver strength: normal/weak
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 8192 cycles/64ms
  - Average refresh period
    - 7.8μs at 0℃ ≤ TC ≤ +85℃
    - 3.9s at +85℃ < TC +95℃

MST7A08D16DMFC is a Multi Chip Package Memory which combines 256Mbit NAND Flash Memory and 512Mbit DDR2 Synchronous Dynamic RAM. 256MB NAND Flash Memory is organized as 32M x 8bits and 512MB DDR2 SDR is organized as 8M x 16bits x 4Banks. In 256Mbit NAND Flash, its NAND cell provides the most cost effective solution for the solid state mass storage market. A program operation can be performed in typical 200μs on the 528-byte Page and an erase operation can be performed in typical 2ms on a 16K-byte block. Data in the page can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. In 512Mbit DDR2 SDR, Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications. MST7A08D16 DMFC is available in 104-ball FBGA Type.
PIN CONFIGURATION (9x9mm, 104-FBGA)
Package Drawing (9x9mm, 104-FBGA)

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. POST REFLOW SOLDER BALL DIAMETER.
   (Pre Reflow Diameter: 0.350±0.02)
3. TOLERANCE INCLUDES WARPAGE.
## PIN DESCRIPTION -104-FBGA

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Function (DDR SDRAM)</th>
<th>Pin Name</th>
<th>Function (NAND Flash)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0~A12</td>
<td>Address Inputs</td>
<td>IO0~IO7</td>
<td>Input and Output</td>
</tr>
<tr>
<td>BA0, BA1</td>
<td>Block Select Address</td>
<td>CE#</td>
<td>Chip Enable</td>
</tr>
<tr>
<td>DQ0~DQ15</td>
<td>Data Input/Output</td>
<td>WEn#</td>
<td>Write Enable</td>
</tr>
<tr>
<td>LDQS, UDQS</td>
<td>Input and Output Data Strobe</td>
<td>RE#</td>
<td>Read Enable</td>
</tr>
<tr>
<td>CS#</td>
<td>Chip Select</td>
<td>ALE</td>
<td>Address Latch Enable</td>
</tr>
<tr>
<td>RAS#</td>
<td>Row Address Strobe Command</td>
<td>CLE</td>
<td>Command Latch Enable</td>
</tr>
<tr>
<td>CAS#</td>
<td>Column Address Strobe Command</td>
<td>WP#</td>
<td>Write Protect</td>
</tr>
<tr>
<td>WEd#</td>
<td>Write Enable</td>
<td>R/B#</td>
<td>Ready/Busy</td>
</tr>
<tr>
<td>LDM, UDM</td>
<td>Input Mask</td>
<td>PRE</td>
<td>Power On-Read Enable, Lock Unlock</td>
</tr>
<tr>
<td>CLK</td>
<td>Clock Input</td>
<td>VCC</td>
<td>Power Supply</td>
</tr>
<tr>
<td>CLK#</td>
<td>Differential Clock Input</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CKE</td>
<td>Clock Enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VREF</td>
<td>Input Reference Voltage</td>
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<td></td>
</tr>
<tr>
<td>VDD</td>
<td>Power Supply</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDDQ</td>
<td>Power for DQ Circuit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VSSQ</td>
<td>Ground for DQ Circuit</td>
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<td></td>
</tr>
<tr>
<td>ODT</td>
<td>On-Die Terminal Control</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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<thead>
<tr>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>NC</td>
<td>No Connection</td>
</tr>
<tr>
<td>DNU</td>
<td>Do Not Use</td>
</tr>
</tbody>
</table>

Rev 01 / Jun. 2011
PART NUMBERING

ATO Solution Co. Ltd

Product type
7: NAND Flash + DDR2 SDRAM

NAND Flash Density
A: 256Mb

NAND Flash I/O
08: x8

SDRAM Density
D: 512Mb DDR2

SDRAM I/O
16: x16

SDRAM Data rate
53: 533Mbps
66: 667Mbps
80: 800Mbps

NAND Flash speed
5: 50ns

Package
FC: 104-ball FBGA
Halogen free

Generation
M: 1st Generation

Voltage
D: NAND Flash 3.3V,
SDRAM 1.8V

Rev 01 / Jun. 2011